High-Speed A/D Conversion Using a Photonic Implementation of an Error Diffusion Neural Network and Oversampling Techniques

Pankaj K. Das,[1] Barry L. Shoop, and Daniel M. Litynski [2]
Photonics Research Center and
Department of Electrical Engineering and Computer Science
United States Military Academy
West Point, New York 10996

Abstract

A fast and accurate A/D converter is the most important component for the connection between the real life applications and the information age revolution. The computer processing speed has gone up by leaps and bounds making the information revolution a reality. However, A/D conversion speed has not kept up and is still a main bottleneck. In this paper, we review the state-of-the-art A/D converters with electronic and photonic technologies including oversampling and parallel processing techniques. A particularly promising approach incorporating a neural network architecture and oversampling error diffusion A/D converter and using a photonic implementation is described in detail. The results of its implementation using smart pixel technology incorporating multiple quantum well (MQW) modulators and CMOS VLSI technology are presented. The potential of this new approach to deliver both high-speed and high-resolution is also analyzed.

1 Introduction

The world has become digital and it is projected that it will become even more so. The relentless advances in computer speed fueled by nearly doubling of size and speed of VLSI circuits every two years is expected to make the information technology revolution in the near future. This is expected to have an impact on society surpassing the similar effect produced by the industrial revolution in the last century. However, many aspects of the world are still analog and thus in many cases a very fast and accurate analog-to-digital (A/D) converter is the last element which is holding up this digital revolution for many systems like all digital radio and TV, radar, etc. The electronic A/D converters have progressed significantly [3, 9]. For an example, using very high frequency transistors like GaAs, HBT, InPDHBT, and others, one has achieved a few gigahertz sampling rate with 4 bit resolution. To achieve 100 GHz bandwidth with 4 or 8 bit resolution it is expected that the electronic solution is not a near term one although one cannot rule out completely an electronic solution. So it is natural to look for some alternative approach: photonic, quantum optic or other mechanism which might lead to a solution in the near future. It is well known that optics or photonics provide extremely high speed (THz sampling rate is practical using femtosecond pulses) and enormous parallelism. However, optical analog processing cannot provide the high dynamic range and linearity needed for many applications. It appears that oversampled A/D converter architectures can provide effective large dynamic range by trading high sampling rate with more number of bits [10] - [14]. One can augment the performance of the oversampled A/D converter further by using parallelism.

Faster device speed increases the sampling rate of an A/D converter. However, device speed by itself does not determine the actual bandwidth as interconnect parasitics and architecture (number of parallel loads) come into play for actual devices. Device speed is related to the unity-gain cut-off frequency, f_T, which is also dependent on its breakdown voltage. Indium phosphide double heterojunction bipolar transistors (InPDHBT) appear to have the best performance compared to InPHBT, GaAs HBT, SiGe HBT, and Si BJT. Each technology has $f_T = 100$ GHz but for InPDHBT, the cut-off voltage at $f_T = 100$ GHz is the highest at approximately 17 V. Using this technology, it is expected that 10-bit 3 Gsps monolithic A/D converters will be developed. Using GaAs HBT technology, 8 bit 2.8 Gsps A/D converters have been demonstrated. Even 10 Gsps converters are possible to implement if one does not demand more than a few bits of accuracy. Compared to the processing speed of computers, A/D converters must have not only the sampling rate but also the resolution *i. e.* the number of bits achievable at a given sampling rate. For example Figure 1 shows the trend in SNRbits over time versus sampling rate as reported by Walden. We observe that over the last 8 years performance of A/D converters has improved by only 1.5 bits for high-performance applications.

[1] P. K. Das is Adjunct Professor at UCSD, San Diego, CA and Emeritus Professor at RPI, Troy, NY.
[2] D. M. Litynski is Professor and Dean of Engineering & Applied Sciences at Western Michigan University, Kalamazoo, MI.

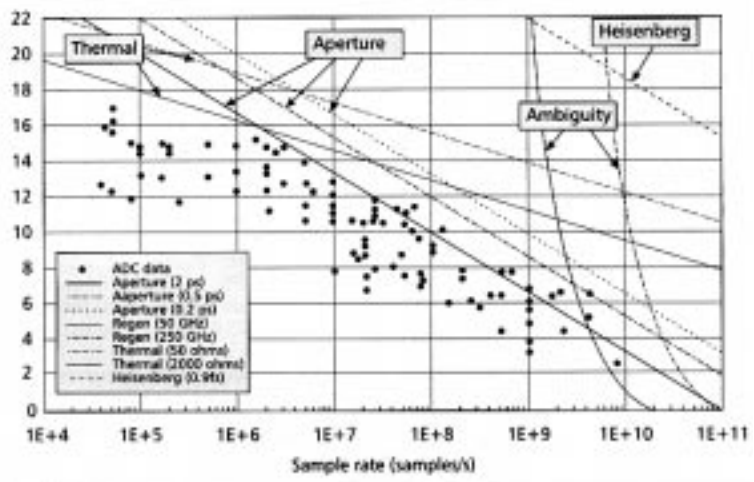

Figure 1: Trends in analog-to-digital converters (from Reference [3]).

As a result, there has recently been a renewed interest in new and innovative approaches to A/D conversion with significant emphasis on photonic techniques. The potential advantages of using photonics technology come in the form of high-speed clocking, broadband sampling, reduced mutual interference of signals and compatibility with existing photonic-based systems. Another advantage of processing signals in the optical domain is the parallelism obtained by performing signal processing in both space and time domains simultaneously. Photonic approaches to A/D conversion have been considered in the past with varying degrees of success. Some of the approaches employed Mach-Zehnder interferometers, other incorporated acousto-optic modulators, and recently multiple quantum well modulators have been incorporated into non-traditional architectures. In this paper, we propose a new technique which uses optical space-time processing. This new technique involves the conversion of oversampled time-domain data into space-domain data using wide-bandwidth modulators or diffractive elements. The spatial signal is then processed in a fashion similar to image processing using digital halftoning and spatial error diffusion filtering using a neural network architecture. In the next section, we discuss characteristics and approaches to A/D conversion. This is followed by the proposed photonic implementation.

2 Analog-to-Digital Conversion

Analog-to-digital conversion is the process by which a continuous-time, continuous-amplitude signal is converted to a discrete-time, discrete-amplitude or digital signal. This process typically employs the four distinct functions shown in Figure 2.

We can describe the overall operation of the generic A/D converter by following a signal as it progresses through each element in Figure 2. The analog input signal $x(t)$ is first bandlimited to the range $0 \leq f_x \leq f_B$ (Hz) by an analog filter to ensure protection against aliasing that could occur during the subsequent sampling operation. The sampling operation in a conventional Nyquist-rate A/D converter is chosen to satisfy the minimum Nyquist criterion: $f_S = f_N = 2f_B$, where f_S is the sampling frequency, f_N is the Nyquist frequency, and f_B is the constrained signal bandwidth. Oversampling is another alternative in which $f_S \gg f_N$ and

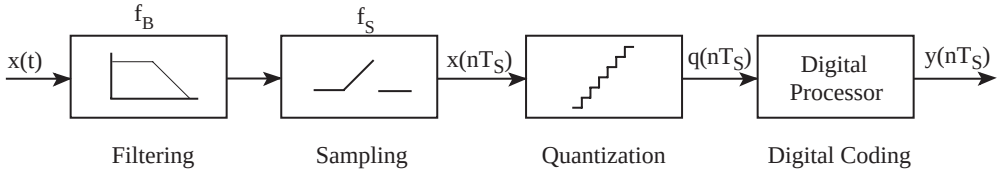

Figure 2: Generic analog-to-digital converter block diagram.

subsequent signal processing techniques are used to provide an advantage. The output from the sampler is $x_n \equiv x(nT_S)$ where T_S is the uniform sampling period $T_S = 1/f_S$. The scalar quantization process maps each continuous-amplitude input x_n to one value in a discrete-amplitude ensemble $q_n \equiv q(nT_S)$. Based on the results of this mapping, the digital processor subsequently generates the digital code of the level that most closely approximates the input analog signal value. The output $y_n \equiv y(nT_S)$ is then the multi-bit, digital word representing the input analog input value.

Although there are several different approaches to quantization in an A/D converter which are typically associated with the quantizer step size, uniform quantizers are one of most practical importance. For this case, quantizers accomplish quantization using 2^b equal quantization steps to achieve b-bits of A/D conversion resolution.

An A/D converter is typically characterized by the sampling rate, conversion rate, and the resolution. The sampling rate for the vast majority of A/D converters is determined according to the minimum Nyquist criterion. There are, however, other types of A/D converter architectures that employ sampling rates that differ from that specified by the Nyquist criterion. Subsampling techniques, which sample the input signal at a rate lower than that specified by the Nyquist criterion, can be employed in applications where the input analog signal is known to be repetitive. In this case, the A/D converter samples the input analog signal such that after multiple cycles of the input, sufficient samples have been obtained to meet the Nyquist criterion and ensure that the required amplitude conversion accuracy has been achieved. Subsampling A/D converters are relatively low conversion rate converters used for applications such as digital multimeters. Oversampling A/D converters [1] such as Delta-Sigma ($\Delta\Sigma$), Sigma-Delta ($\Sigma\Delta$), or error diffusion modulators, instead sample the input analog signal at rates which are typically much higher than that required by the Nyquist criterion. In this case, linear filtering and signal processing techniques are employed to improve the overall performance of the A/D converter. Oversampling A/D converters fundamentally trade sampling bandwidth for improved amplitude resolution. Here, a low resolution quantizer and a linear filter are embedded in a feedback architecture in order to spectrally shape the quantization error resulting from a low-resolution quantizer. This spectral noise shaping forces the quantization noise to frequencies above the baseband information bandwidth. In a subsequent operation, a digital postprocessor removes the spectrally-shaped noise and decimates the resulting digital output, thereby improving the overall signal-to-quantization noise ration (SQNR) and converter performance and providing the high-resolution digital representation at the Nyquist conversion rate of the input signal.

The ultimate resolution of the A/D converter is limited by thermal noise, quantization noise, sampling jitter, comparator ambiguity, and quantizer hysteresis [3]. It is customary to define a measure, called the effective number of bits resolution or b_{eff}, for each of these processes. It turns-out that for each process this oversampling ratio dramatically aides in extending this b_{eff} as detailed below. This is very important as with the photonic sampling one can achieve a very high oversampling ratio.

Thermal noise reduces the overall dynamic performance of an A/D converter in much the same way it does in any other system. The upper-bound on the effective number of bits resolution due to thermal noise only is given by

$$b_{eff} = \frac{1}{2}\log_2\left(\frac{M}{3kTR_{eff}f_B}\right) - 0.292. \tag{1}$$

The oversampling A/D converter provides an improvement in thermal noise performance proportional to the oversampling ratio, yielding an increase of 1-bit for every doubling of the oversampling ratio. The effective number of bits resolution for quantization noise only is given by

$$b_{eff} = \log_2\left[\frac{\sqrt{2N+1}}{\pi^N}\cdot M^{(N+\frac{1}{2})}\right]. \tag{2}$$

When considering quantizer noise, the oversampling A/D converter effectively provides an additional $N + \frac{1}{2}$ bits of resolution for every doubling of the oversampling ratio. Here, N is the order of the feedback filter and consequently the order of the oversampling modulator.

Sampling jitter in an A/D converter results in nonuniform sampling of the input signal which subsequently results in an additional error contribution thereby increasing the total error power in the quantizer output. The magnitude of this error is a function of both the statistical properties of the sampling jitter and the input signal itself. In an oversampled A/D converter, there are two distinctly different approaches to accomplishing signal sampling: explicit sampling and integral sampling. Explicit sampling is defined here as an explicit

sampling operation subsequent to the anti-alias filtering operation. Integral sampling describes the sampling function when performed by the quantizer or within the oversampling modulator. Integrated sampling simplifies the overall A/D converter architecture by eliminating the need for separate sampling circuitry and, as will be shown shortly, reduces the impact of sampling jitter on the overall performance of the oversampling A/D converter. It is assumed that the sampling uncertainty is an uncorrelated Gaussian random process with standard deviation τ_j. For explicit sampling, one obtains

$$b_{eff} = \frac{1}{2}\log_2\left[\frac{M}{(2\pi f_x \tau_j)^2}\right] - 0.292. \tag{3}$$

effective number of bits resolution. As with thermal noise, an increase of 1-bit resolution for every doubling of the oversampling ratio results for explicit sampling jitter performance. If the sampling is performed instead as an integral part of the oversampled modulator, the impact from sampling uncertainty is fundamentally different. In this case, the sampling occurs as part of the quantization process and therefore, the noise shaping characteristics of the modulator modify the spectral contribution of the sampling jitter error in much the same way the modulator spectrally shapes the quantization noise. For this case, one obtains

$$b_{eff} = \log_2\left[\frac{\sqrt{2N+1}\cdot M^{(N+\frac{1}{2})}}{\pi^N}\right] + 3.012\log_2\left[\frac{1}{(2\pi f_s \tau_j)^2}\right] \tag{4}$$

effective number of bits resolution. For an oversampling ratio of $M = 10^3$ and a second-order error diffusion filter $N = 2$, Eq. (4) predicts an improvement of 22 bits over the sampling jitter performance for explicit sampling. The oversampling A/D converter is therefore insensitive to sampling jitter resulting from integral sampling.

Quantizer hysteresis is another common source of error in comparators used for quantization. The hysteresis error is modeled as an additive white noise source with power $S_h = (h\Delta/2)^2$, where h is the magnitude of the quantizer hysteresis relative to the quantizer step size Δ. This noise undergoes the same spectral noise shaping as the quantization noise and the integral sampling jitter resulting in

$$b_{eff} = 1.65(N + 0.258) + \log_2\left[\frac{\sqrt{N+1}\, M^{N+\frac{1}{2}}}{h}\right]. \tag{5}$$

Since the hysteresis error contribution is within the modulator, it is suppressed by the noise shaping characteristic of the feedback loop.

Comparator ambiguity results from the finite speed of response of the comparator to a small input. Since the comparator in an oversampled A/D converter is embedded within the noise shaping feedback loop, the Nyquist-rate results can be extended to ovesampling architectures by recognizing that the comparator ambiguity noise contribution will be spectrally shaped by the noise shaping characteristic of the oversampling modulator in the same way as the quantization noise, integrated sampling jitter, and hysteresis. Again, the oversampling architecture results in an additional $N + \frac{1}{2}$ bits of resolution for every doubling of the oversampling ratio.

3 Photonic Oversampled A/D Conversion Using Digital Halftoning

As mentioned previously, optics and photonics provide extremely high speed (THz sampling rate is practical using femtosecond pulses) and enormous parallelism. However, optical analog processing cannot provide the dynamic range and linearity needed for many applications. It appears that oversampled A/D converter architecture can provide effective large dynamic range by trading high sampling rate for increased amplitude resolution and consequently a larger number of bits.

A parallel implementation of the oversampled A/D converter is shown in Figure 3. Here, $x(nT)$ represents the n^{th} sampled signal and T is the sampling time. In place of processing the signal using a single sigma-delta modulator, the signal is split N-wise and then applied to N separate modulators. At the output of

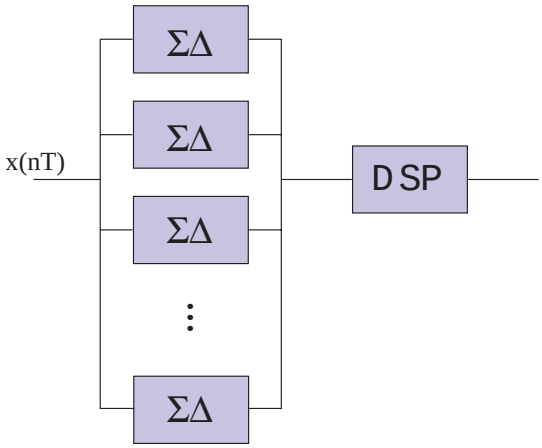

Figure 3: Channelized ΣΔ A/D conversion.

each modulator, the signal voltage adds coherently. However, the quantization noise being incoherent due to the presence of noise, adds in power only. This produces 3 dB improvement in SNR for each doubling of the number of channels. This is equivalent to 1/2-bit improvement in the effective number of bits for each doubling of the number of channels. This parallel architecture has been well known in the CMOS A/D community. However, as it involves a large amount of real-estate in the silicon wafer, it is quite impractical for a CMOS implementation.

Consider the simplest optical implementation shown in Figure 4 where the signal modulates a high speed electrooptic modulator. The sampling optical pulse thus becomes the input $x(nT)$ which is placed at the focal plane of a lens. The expanded light is incident on the $N \times N$ photodetector array. The electrical output of this array can be the input to the $N \times N$ modulators. For the simple 1-bit oversampled A/D converter, the modulator implementation involves just a thresholding operation and can be performed using smart pixels. Also, it is important to note that the incident light beam on the $N \times N$ photodetector array is equivalent to the image of the sampled light and if one performs only one-bit thresholding operation, it becomes nothing but digital halftone of an uniform image. Using error diffusion and smart pixel technology, this implementation becomes quite simple and practical. For the case of no error diffusion, the output of all the detectors are to be summed-up and postprocessed. The postprocessing involves a digital low-pass filter and an electronic low-bandwidth digital converter. If we consider a typical case of 1024×1024 photodetector array, we obtain an 10-bit improvement in accuracy.

It is of interest to consider the performance bounds for this simple photonic implementation. We should consider two cases: (a) $x(nT)$ is sampled at Nyquist rate; (b) $x(nT)$ is sampled at M times the Nyquist rate, i.e., the oversampling ratio (in time) is M. For the first case $N \times N$ parallel operation acts like an A/D converter with oversampling ratio $M = N \times N$. Thus for this case the performance bound due to thermal, sampling jitter and comparator hysteresis, will be the same as discussed in the last section. One should add shot noise for the optical implementation. We should also consider the effect of mismatch between the

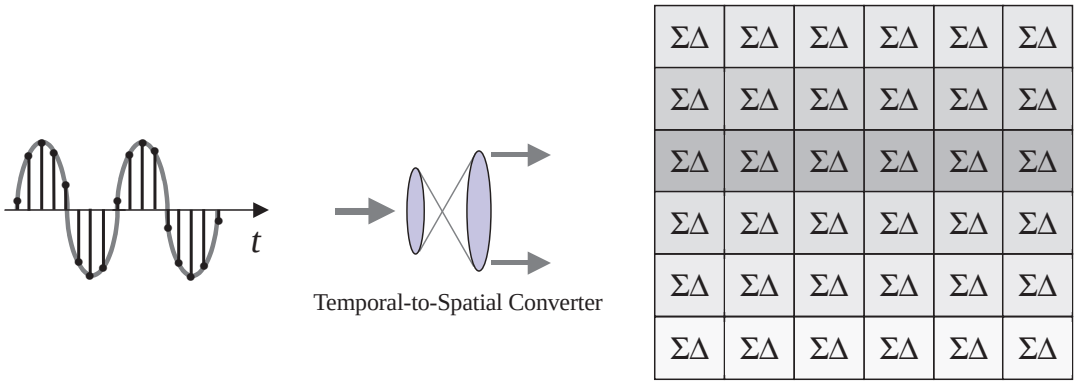

Figure 4: Photonic approach to distributed oversampled A/D conversion.

parallel channels as it is expected that there will be variations in the performance of the detectors and the threshold level of quantizers. If we model these variations as random, they will appear as equivalent to random dithering. For this case one has

$$SNR_{P(\Sigma\Delta)} = SNR_{1(\Sigma\Delta)} \cdot \frac{P}{(1 + \frac{\delta^2}{\Delta^2})}, \tag{6}$$

where P is the number f parallel channels, $SNR_{1(\Sigma\Delta)}$ is the SNR associated with a single $\Sigma\Delta$ modulator, and δ represents the statistical difference in quantizer step sizes over the P channels.

For the case (b), we have oversampling due to time M and oversampling due to space $N \times N$. Thus the effective oversampling ratio is $M \times N \times N$. In the absence of any error diffusion or feedback structure of sigma-delta modulator, the results will be the same as that discussed above where effective oversampling ratio is used.

To include spatial error diffusion, one needs to modify the structure shown in Figure 4. One possibility is to use a serial to parallel converter. Very fast serial to parallel converters can be implemented using femtosecond optical time to space converters. For this case, different rows have the same $x(nT)$ giving us space oversampling, but different columns have different $x(nT)$. Thus for this case, one can use error diffusion between columns as in the case of digital image halftoning. Here, the effective number of bits will be quite large for higher order systems as discussed in Section 5. Unfortunately for this case the effect due to mismatch between the rows is quite severe as the aliasing effect needs to be considered. This mismatch effect, however, is significantly reduced for large M.

We have discussed a simple practical photonic implementation of parallel oversampled A/D converter. This implementation can increase the effective number of bits significantly and quite robustly. Using micro-mechanical structures and smart-pixel technology, the proposed implementation will advance the high end A/D converter performance enormously.

4 Femtosecond Serial-to-Parallel Demultiplexing and Its Application to Oversampled A/D Conversion

Optics provides high speed and parallelism. For an example, femtosecond pulses can be routinely produced and manipulated leading to multi-terabit rates. However, the final product or application will always involve electronics at the end. Electronics, although following Moore's Law will approach tens of gigabit per sec, it is not expected to reach terabit in the near future. Thus to use optical terabit in practical systems one must have some mechanism or technique to couple the optical high speed to electronic slower speed. This can be done using serial to parallel converters. These devices are also known as optical time to space and space to time processors, interleavers using commutators and multirate fibers, N-path filters. These devices can be implemented using different optical techniques.

One particular case where these devices can be used is in oversampled A/D converter which is implemented using photonics rather than conventional CMOS. As discussed earlier, in an oversampling A/D converter, a low-resolution quantizer is embedded in a feedback architecture in order to reduce the quantization noise through spectral noise shaping, effectively trading bandwidth for improved amplitude resolution. Here, a large error associated with a single sample is diffused over many subsequent samples after which linear filtering techniques remove the spectrally- shaped noise, thereby improving the overall SNR of the converter. The purpose of this section is two-fold: (a) to discuss the use of time-interleavers to increase the performance of high resolution, high speed photonic based A/D conversion architectures, and (b) to consider a new architecture which involves both space and time processing and parallels digital halftoning of images. The practical issue of performance degradation due to mismatch is also discussed.

Figure 5 shows the overall systems diagram. The serial to parallel converters can be implemented using many different techniques to be discussed shortly. If the serial to parallel conversion ratio is N, then the electronic converter speed needs to be f/N. For example, if the sampling speed is 64×10^9 and $N = 64$, the electronic A/D converter needs to be operating at 1.0 GHz.

Use of time-interleavers to increase the overall sampling rate is well-known in CMOS VLSI community [7, 8]. One can use block filters with a commutator to work in the time domain or use multirate subband filters with a commutator to work in the frequency domain. However, in this paper we are interested in

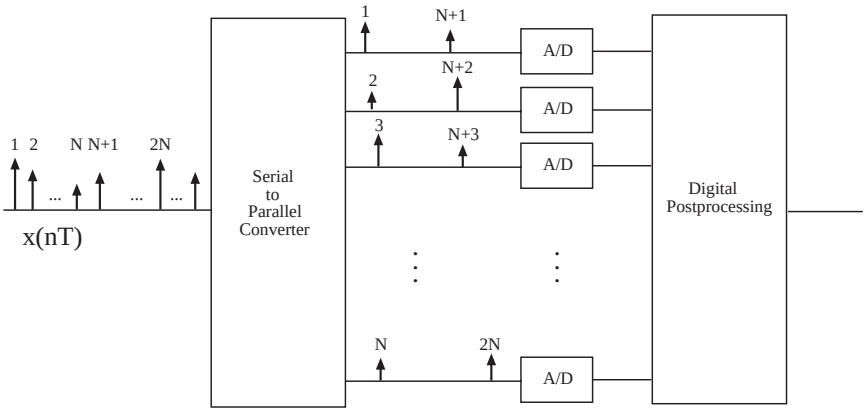

Figure 5: System diagram for high-resolution photonic A/D converter.

the photonic implementation of the time-interleaver [4] - [6], the frequency-domain implementation will be discussed in a separate paper.

One of the best optical implementations of serial to parallel demultiplexer is shown in Figure 6 where the signal pulse train is multiplied by a chirp waveform in time and then using a wavelength division multiplexing (WDM) device, the pulses can be demultiplexed into different channels. The chirp signal can be generated in many ways - one can use a diffraction grating, prism, linearly dispersive element like a dispersive fiber, as well as others, all in conjunction with a femtosecond pulse. Another approach is to use tunable laser sources like a semiconductor laser where the output wavelength varies linearly with time. Note that the chirp used need not be continuous but can also be discrete.

The WDM or wavelength selective devices can be an array waveguide (AWG), tunable Fabry-Perot, or any other WDM device which are currently being used in optical fiber communication systems. Note, however, that this method does not preserve phase. Another technique is to use so-called time-space conversion which uses a nonlinear crystal. For this case, phase information is maintained. Finally, one can use Mach-Zehnder switches to perform two-fold time interleaving. This can then be repeated N times to achieve 2^N-fold serial-to-parallel conversion.

Although many possibilities exist for implementing the A/D converter, we consider here a particular case which involves digital halftoning and a smart pixel architecture. This approach is shown in Figure 7 where using micro lenses the time-interleaved pulses are spread over P detectors in parallel. This is the architecture which uses both time and space processing.

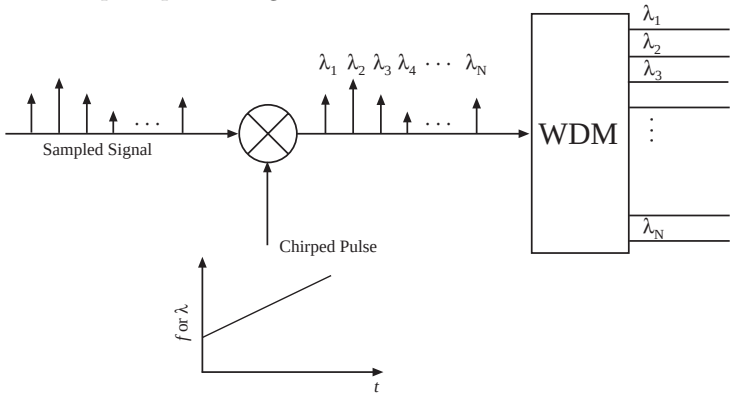

Figure 6: Schematic of a photonic serial-to-parallel converter using a chirped pulse and WDM device.

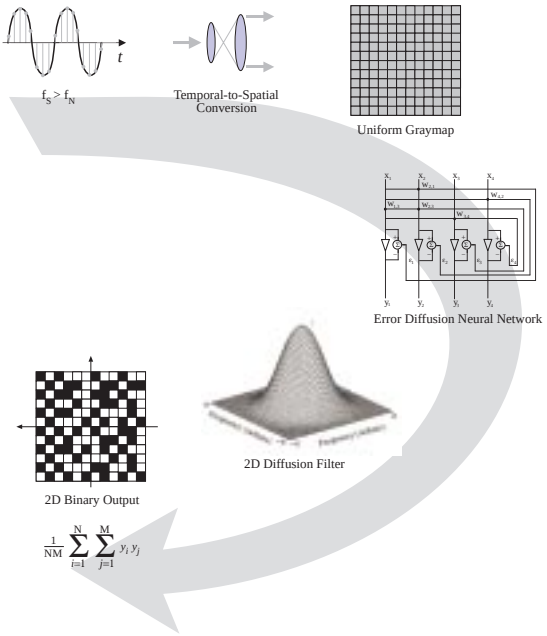

Figure 7: System diagram for a high-resolution A/D converter based on temporal and spatial oversampling and an error diffusion neural network architecture.

5 Oversampled A/D Conversion, Digital Image Halftoning, and Neural Network Processing

Oversampled A/D conversion, most commonly referred to as $\Sigma-\Delta$ or $\Delta-\Sigma$-modulation, is an A/D technique which has become popular in the audio industry. This approach relies on a temporal form of error diffusion coding, whereby a large error associated with a single sample is diffused over many subsequent samples. Here, the error is generated by a low-resolution quantizer, and the diffusion is implemented by embedding the quantizer and a linear filter in a feedback architecture. Figure 8 shows a generalized block diagram of an oversampled A/D converter. The analog signal $x(t)$ is first bandlimited to the range $0 \leq f_x \leq f_B$ (Hz) and is then sampled at a rate $f_S \gg f_N$, where f_S is the sampling frequency, f_N is the Nyquist frequency of the sampled signal, and f_B is the constrained signal bandwidth. The output of the sampler is then input to the modulator, which provides coarse amplitude quantization and spectral shaping of the quantization noise. The digital postprocessor, which consists of a digital low pass filter and decimation circuitry, removes the quantization noise which was spectrally shaped by the modulator, provides anti-aliasing protection, and reduces the rate to the original sampled signal's Nyquist rate by trading word rate for word length.

The modulator is the key element of this architecture whose function is to quantize the analog input signal and reduce the quantization noise within the signal baseband. For optical implementations, an alternative architecture to those typically associated with electronic implementations is used in order to reduce optical losses and prevent quantizer overload. Figure 9 shows the block diagram of this specific realization called a

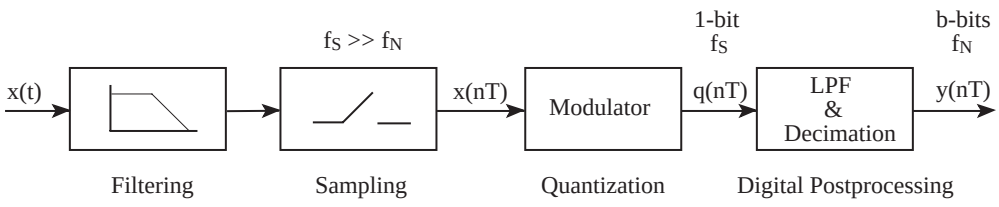

Figure 8: Generalized block diagram of an oversampled A/D converter.

recursive error diffusion modulator.

Here, $H(z)$ represents the z-transform of a causal, unity gain filter, z^{-1} is a unit sample delay, and q is a low-resolution quantizer. Figure 10 shows the noise shaping characteristics for first- and second-order noise shaping filters where $H(z) = 1$ and $H(z) = 1 - 2z^{-1} + z^{-2}$, respectively.

A convenient measure by which to compare an A/D converter's performance is the maximum signal-to-quantization noise ratio, $SQNR_{max}$ which is defined as the ratio of the output power at the frequency of a full-scale input sinusoid to the quantization noise power within the signal baseband. In the case of an oversampled A/D converter, analytic evaluation of this expression requires knowledge of the quantizer error spectrum and the postprocessor filter transfer function. If we assume white quantization noise characteristics and an ideal low pass filter with cutoff frequency f_B, the $SQNR_{max}$ for an N^{th}-order modulator with a full-scale input range of $\pm\Delta/2$ can be shown to be

$$SQNR_{max}(M, N) = \frac{3}{2} \cdot \left[\frac{2N+1}{\pi^{2N}}\right] \cdot M^{2N+1}, \tag{7}$$

where $M = f_S/f_N$ is defined as the oversampling ratio and N is the filter order. From Equation(7), the effective number of bits resolution can be described as

$$b_{eff} = \frac{1}{2}\log_2\left[\frac{2N+1}{\pi^2 N} \cdot M^{2N+1}\right]. \tag{8}$$

A conventional uniform Nyquist rate quantizer with b-bits resolution can be shown to provide a $SQNR_{max} = 3 \cdot 2^{2b-1}$ [2]. Figure 11 shows the theoretical $SQNR_{max}(M, N)$ and equivalent resolution for first- through fourth-order oversampled modulators as a function of oversampling ratio. Results for $N = 1$ are also included because, although the additive noise model does not predict the spectral characteristics of the quantization noise, it does yield accurate results for the $SQNR_{max}$. The case of no noise shaping represents the $SQNR_{max}$ that can be expected if the same quantizer, embedded in the feedback loop of the oversampled modulator, were simply oversampled and digitally filtered. The slope of this curve is 3dB per octave while those of the $N = 1$ and $N = 2$ curves are 9 dB and 15 dB, respectively, showing the significant advantage achieved by using a noise shaping modulator.

Digital image halftoning is an important class of A/D converter which can be considered the spatial counterpart of temporal oversampled A/D conversion. In digital halftoning, a continuous-tone input image is first spatially oversampled to produce an image with many more pixels than that required by the Nyquist criterion. This oversampled image is then processed to produce an output image which is strictly bilevel. The choice of the binary output values is judiciously chosen such that the resulting halftoned image creates the illusion of a continuous-tone image. To improve the halftone image quality, a method of quantization is used in which the error associated with the nonlinear quantization process is diffused within a local region and subsequent filtering techniques employed in an effort to improve some performance metric such as signal-to-noise ratio. Figure 12 shows a block diagram of a typical halftoning process using this error diffusion algorithm. It is clear that this block diagram is the spatial equivalent of the temporal error diffusion architecture of Figure 9. Note that W in this figure is derived from the original error diffusion weights which are used in $H(z)$ in Figure 9.

We are currently investigating an optoelectronic implementation of the error diffusion neural network using smart pixel technology. Smart pixel technology integrates optoelectronic devices for the input and

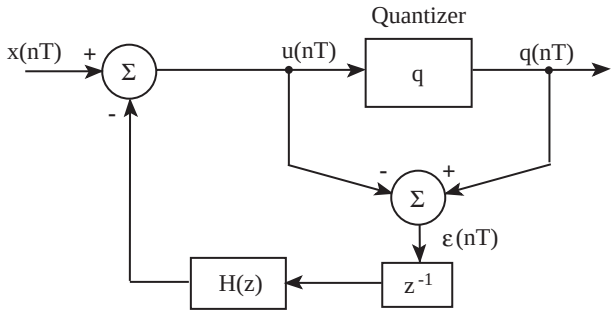

Figure 9: Block diagram of a recursive error diffusion modulator.

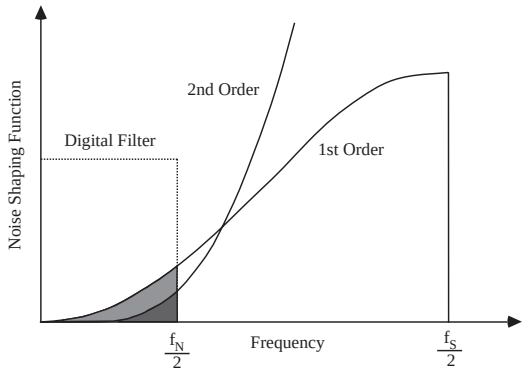

Figure 10: Noise shaping characteristics for first- and second-order filters.

output functionality with electronic circuitry for the processing functionality. A smart pixel hardware implementation of the error diffusion neural network provides the potential to simultaneously leverage the computational complexity of electronic circuitry and the parallelism and high-speed switching of optics.

Our new approach to photonic A/D conversion uses a distributed neural network, oversampling techniques, and a smart pixel hardware implementation. In this approach, the input signal is first sampled at a rate higher than that required by the Nyquist criterion and then presented spatially as the input to a two-dimensional error diffusion neural network consisting of $M \times N$ neurons, each representing a pixel in the image space. The neural network processes the input oversampled analog image and produces an $M \times N$ pixel binary or halftoned output image. By design of the neural network, this halftoned output image is an optimum representation of the input analog signal. Upon convergence, the neural network minimizes an energy function representing the frequency-weighted squared error between the input analog image and the output halftoned image. Decimation and low-pass filtering techniques, common to classic one-dimensional oversampling A/D converters, digitally sum and average the $M \times N$ pixel output binary image using high-speed digital electronic circuitry. By employing a two-dimensional smart pixel neural approach to oversampling A/D conversion, each pixel constitutes a simple oversampling modulator thereby producing a distributed A/D architecture, shown in Figure 13. Spectral noise shaping across the array diffuses quantization error thereby improving overall SNR performance. Here, each quantizer within the network is embedded in a fully-connected, distributed mesh feedback loop which spectrally shapes the overall quantization noise thereby significantly reducing the effects of component mismatch typically associated with parallel or channelized A/D approaches. The two-dimensional neural array provides higher aggregate bit rates which can extend the useful bandwidth of photonic-based, oversampling A/D converters. The performance of this distributed approach to A/D conversion can be described in several different ways. The SQNR for this architecture was given previously by Equation(7). This equation describes the performance of an Nth-order oversampling modulator, part of an oversampling A/D converter. The difference here is that the oversampling

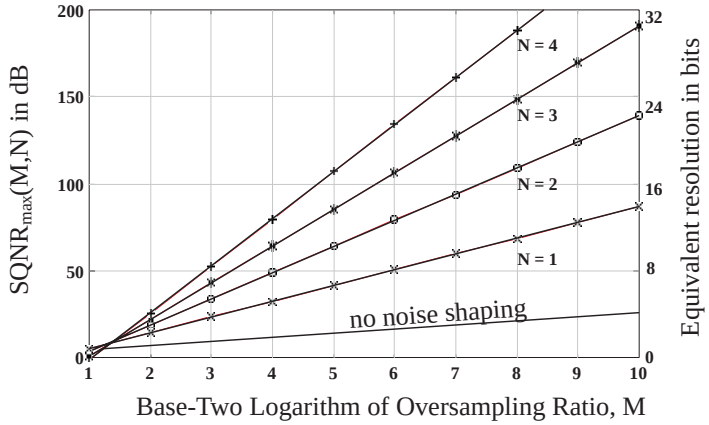

Figure 11: Maximum signal-to-quantization noise ratio of N^{th}-order oversampling modulators.

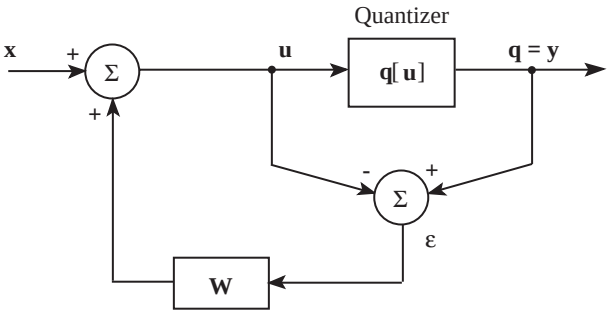

Figure 12: Block diagram of a 2-D recursive error diffusion architecture.

ratio is proportional to the output image size and therefore can be larger than classical oversampling ratios. Component mismatch effect tolerance can be quantified by considering the error diffusion neural network performance under these conditions. As an example, the effect of threshold mismatch across the array can be characterized as a modification to the neural network energy function according to

$$E = (\mathbf{y} - \mathbf{x})^T \mathbf{A}(\mathbf{y} - \mathbf{x}) + \varepsilon_t^T \mathbf{A}^{-1} \varepsilon_t - 2\varepsilon_t^T (\mathbf{y} - \mathbf{x}), \tag{9}$$

where ε_t is a vector containing the threshold mismatch of the array. This first term in Equation (9) is the same as in the original error diffusion neural network. The last two terms are contributions from threshold mismatch. The matrix $\mathbf{A}$ is derived from the error diffusion filter weights and has high-pass spectral characteristics. Equation (9) demonstrates that the contribution of the threshold mismatch to performance is spectrally-shaped by the error diffusion filter thereby reducing the overall impact.

In contrast to the majority of current smart pixel research, the architecture reported here is a mixed signal application of smart pixel technology. The optoelectronic circuitry for a proof-of-concept 5×5 error diffusion neural network was implemented in 0.5 μm silicon CMOS technology requiring the functionality of one-bit quantization, subtraction, neuron-to-neuron weighting and interconnection, and optical input and output. The circuitry associated with the neurons of this error diffusion neural network is implemented using CMOS-SEED smart pixel technology. The one-bit quantizer is implemented using a wide-range transconductance amplifier operated in the subthreshold regime. The slope of this sigmoidal function was carefully designed by matching MOSFET transistors to meet the convergence criteria and the nonlinear dynamics of the error diffusion neural network. All state variables in this circuit are represented as currents and therefore the subtraction functionality was implemented using current summation techniques at specified nodes. The error weighting and distribution circuitry for the 5×5 array was implemented in silicon circuitry by designing and matching the width-to-length ratios of both the individual and stage-to-stage MOSFET transistors. Bi-directional error currents were implemented to provide the circuitry and the network with fully-symmetric performance. Optical input and output to each neuron was implemented using SEED multiple quantum

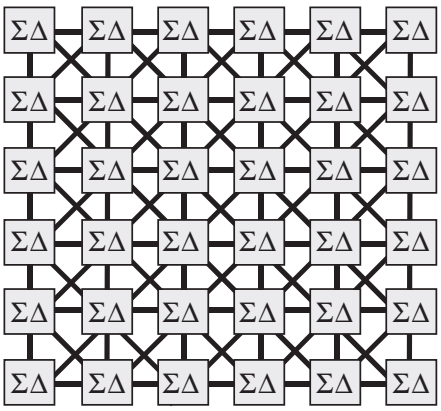

Figure 13: Fully-connected, distributed oversampling A/D converter architecture.

well (MQW) modulators. The input MQW is reverse-biased and functions as an optical detector while the output optical binary signal is produced using a forward biased MQW, which provides photoemission through electroluminescence. The central neuron of the smart pixel array consists of approximately 160 transistors while the complete 5×5 array accounts for over 3600 transistors. The central neuron is interconnected to the surrounding 24 neurons in the 5×5 array using a fixed interconnect and weighting scheme. SPICE simulations of each of the functional components as well as the complete 5×5 nonlinear dynamical neural network were performed using transistor parameters extracted from a previous 0.5mm MOSIS foundry run and have verified both functional operation as well as overall network performance. Individual component functionality was experimentally characterized and dynamic operation of the full 5×5 neural array was also experimentally characterized. Dynamic stimulus of single and multiple neurons was also conducted and demonstrated correct error diffusion and network operation.

Acknowledgments. This research was supported by the Army Research Office and the Defense Advanced Research Projects Agency under the Photonic A/D Converter Technology Project.

References

[1] H. Inose and Y. Yasuda, "A unity bit coding method by negative feedback," *Proc. IEEE*, vol. 51, pp. 1524-1535, 1963.

[2] W. Bennett, "Spectra of quantized signals," *Bell Syst. Tech. J.*, vol. 27, pp. 446–472, 1948.

[3] R. H. Walden, "Analog-to-digital converter survey and analysis," *IEEE J. Select Area of Communications*, vol. 17, pp. 539–550, 1999.

[4] C. DeCusatis and P. Das, "Spread spectrum techniques in optical communication using transform domain processing," *IEEE J. Select Area of Communications*, vol. 8, pp. 1608–1616, 1990.

[5] J. S. Salehi, A. M. Weiner and J. P. Heritage, "Coherent ultrashort pulse code division multiple access communication systems," *IEEE J. Lightwave Tech,*, vol. 8, pp. 478–491, 1990.

[6] J. Kang, M. Y. Frankel and R. D. Esman, "Highly parallel pulsed opto-electronic analog-to-digital converter," *IEEE Photonics Tech. Letters*, vol. 10, pp. 1626–1628, 1998.

[7] A. Petragalia and S. K. Mitra, "Analysis of mismatch effects among A/D converters in a time-interleaved waveform digitizer," *IEEE Trans. Instrument. and Measurement*, vol. 40, pp. 831–835, 1991.

[8] R. Khorini-Poorfard, L. B. Lim and D. A. Johus, "Time-interleaved oversampling A/D converters: theory and practice," *IEEE Trans. Circuits and Syst.*, vol. 44, pp. 634–645, 1997.

[9] K. Poulton, *et al.*, "A 6 bit 4 Gs/s ADC fabricated in a GaAs HBT process," *GaAs IC Symp. Tech. Digest*, pp. 240–243, 1994.

[10] B. L. Shoop, *Optical oversampled analog-to-digital conversion*, Ph.D. Dissertation, Stanford University, 1992.

[11] B. L. Shoop and J. W. Goodman, "Optical oversampled analog-to-digital conversion," *Applied Optics*, vol. 31, pp. 5654–5660, 1992.

[12] B. L. Shoop, A. H. Sayles, and D. M. Litynski, Chapter 20, "New Devices for Optoelectronics: Smart Pixels," Chapter 20 in *Handbook of Fiber Optic Data Communication*, C. DeCusatis, D. Clement, E. Maass, and R. Lasky, Ed., Academic Press, San Diego, California, pp. 705–758, 1997.

[13] B. L. Shoop, A. H. Sayles, D. A. Hall and E. K. Ressler, "A smart pixel implementation of an error diffusion neural network for digital halftoning," *Invited Paper* in *International J. of Optoelectronics*, vol. 11, pp. 217–228, 1997.

[14] B. L. Shoop, "Photonic analog-to-digital conversion," *Invited Paper* in *Proceedings of the SPIE*, vol. 3490, pp. 252–256, 1998.

[15] B. L. Shoop, P. K. Das, and D. M. Litynski, "Improved resolution A/D converter using oversampling techniques," *Proceedings of the SPIE*, vol. 3643, pp. 192–199, 1998.

[16] T. Kurokawa, H. Tsuda, K. Okamoto, K. Naganuma, H. Takenouchi, Y. Inoue, and M. Ishii, "Time-space conversion optical signal processing using arrayed waveguide gratings," *Electronics Lett.*, vol. 33, pp. 1890–1891, 1999.

[17] P. C. Sun, Y. Mazurenko,, and Y. Fainman, "Femtosecond pulse imaging: ultrafast optical oscilloscope," *J. Opt. Soc. Am. A*, pp. 1159–1170, 1997